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EXAMINER	
KNOLL, CLIFFORD H	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/086,665	APOSTOL ET AL.	
	Examiner	Art Unit	
	Clifford H. Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. *Claims 27-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.*

In claims 27-30, references to "the particular subsystem" lack clear antecedent basis.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. *Claims 1-3, 10-12, 16, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (US 6185520 B1) in view of well-known features, as evidenced by Geusic (US 20010026439 A1).*

Regarding claim 1, Brown discloses a first outbound queue (e.g., Fig. 6, "631") and second outbound queue (e.g., Fig. 6, "632") including a bus arbitration priority (e.g., col. 10, lines 13-15, "shared PCI bus"), a first state machine (e.g., col. 10, lines 28-32) to service queues according to the first and second outbound priorities (e.g., col. 10, lines 23-26), where access is granted at least in part on the included bus arbitration priorities of the contending bus transactions (e.g., col. 10, lines 13-15, "shared PCI bus"). Brown does not expressly mention the bus as on-chip; however the Examiner takes Official Notice that the integration of circuits onto a chip is widely known to improve the speed and performance of the circuits, as evidenced by Geusic (para. 4).

Regarding claim 2, Brown also discloses storing priorities to be accorded in a configuration register (e.g., col. 11, lines 9-15, "target device basis").

Regarding claim 3, Brown also discloses a third outbound queue (e.g., col. 10, lines 27-29) which facilitates selective staging of the outbound bus transactions, where the state machine is also coupled to the third outbound queue to service along with the other outbound queues (e.g., col. 10, line 28, "granularity of prioritization").

Regarding claim 10, Brown discloses core subsystem logic (e.g., col. 6, lines 41-47), a first outbound queue (e.g., Fig. 6, "631") and second outbound queue (e.g., Fig. 6, "632") including a bus arbitration priority (e.g., col. 10, lines 13-15, "shared PCI bus"), a first state machine (e.g., col. 10, lines 28-32) to service queues according to the first and second outbound priorities (e.g., col. 10, lines 23-26), where access is granted at least in part on the included bus arbitration priorities of the contending bus transactions (e.g., col. 10, lines 13-15, "shared PCI bus"). Brown does not expressly mention the

bus as on-chip; however the Examiner takes Official Notice that the integration of circuits onto a chip is widely known to improve the speed and performance of the circuits, as evidenced by Geusic (para. 4).

Regarding claim 11, Brown also discloses storing priorities to be accorded in a configuration register (e.g., col. 11, lines 9-15, "target device basis").

Regarding claim 12, Brown also discloses a third outbound queue (e.g., col. 10, lines 27-29) which facilitates selective staging of the outbound bus transactions, where the state machine is also coupled to the third outbound queue to service along with the other outbound queues (e.g., col. 10, line 28, "granularity of prioritization").

Regarding claim 16, Brown also discloses a collection of peripheral device controllers (e.g., Fig. 5a, "550", "550").

Regarding claim 21, Brown discloses determining intra-subsystem priorities for transactions with other subsystems to be serviced (e.g., col. 10, lines 23-26), generating and staging the transactions in accordance with the determined priorities (e.g., Fig. 6, "631", "632"), including a bus arbitration priority (e.g., col. 10, lines 13-15, "shared PCI bus"), serially servicing the staged transactions in accordance with the priorities (e.g., col. 10, lines 23-26) and requesting access to the bus for each staged transaction (e.g., col. 10, lines 13-15). Brown does not expressly mention the bus as on-chip; however the Examiner takes Official Notice that the integration of circuits onto a chip is widely known to improve the speed and performance of the circuits, as evidenced by Geusic (para. 4).

Regarding claim 22, Brown also discloses the generating and staging in a selected on of a plurality of outbound queues (e.g., col. 10, 26-28) in accordance with the determined intra-system priorities including with each a bus arbitration priority for use to arbitrate access (e.g., col. 10, lines 13-15).

3. *Claims 4-6 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown as applied to respective parent claims, in view of Bergeson (US 6784890 B1).*

Regarding claims 4 and 13, Brown also discloses first and second inbound queues (e.g., col. 12, lines 51-55, "plurality of input queues") at the choosing of originating subsystems each including a bus arbitration priority and being granted access to the bus (e.g., col. 10, lines 37-39, 14, "components ... for both directions") and the second state machine to service certain inbound queues according to first and second priorities (e.g., col. 11-14). While Brown thus expressly mentions first and second inbound queues of the single bus recited, and according priority to inbound queues, he does not expressly mention according priority to inbound queues which pertain to the single bus recited; however, Bergeson discloses this (e.g., Figs. 1b, 2a; col. 3, lines 13-27, adequately teaches according priority to inbound queues). It would have been obvious to one of ordinary skill in the art to combine Bergeson with Brown, because Bergeson teaches the advantage of managing priority on inbound queues (e.g., col. 1, lines 15-21).

Regarding claims 5 and 14, Brown also discloses storing priorities for inbound queues to be accorded in a configuration register (e.g., col. 11, lines 9-15, "initiator device basis").

Regarding claims 6 and 15, Brown also discloses a plurality of inbound queues (e.g., col. 12, lines 51-55, "plurality of input queues") at the choosing of originating subsystems each including a bus arbitration priority and being granted access to the bus (e.g., col. 10, lines 37-39, 14, "components ... for both directions") and the second state machine also coupled to the additional inbound queue. Brown does not expressly mention according priority to the third inbound queues which pertain to the single bus recited, complementing the first and second inbound queue; however, Bergeson discloses this (e.g., Figs. 1b, 2a; col. 3, lines 13-27, adequately teaches according priority to inbound queues). It would have been obvious to one of ordinary skill in the art to combine Bergeson with Brown, because Bergeson teaches the advantage of managing priority on inbound queues (e.g., col. 1, lines 15-21). The plurality of inbound queues disclosed by Brown refers to two or more queues and thus encompasses a third inbound queue, which is not unforeseen, as seen by Brown, who teaches adding further additional queues to the existing two outbound queues to increment the granularity of prioritization (e.g., col. 10, lines 26-28), and by Bergeson, who teaches using three inbound queues, each accorded a priority (e.g., Fig. 2a, "202", "204", "206", col. 3, lines 13-27).

4. Claims 7-9, 17-20, and 23-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown in view of Bergeson, further in view of well-known features, as evidenced by Geusic.

Regarding claim 7, Brown discloses first and second inbound queues (e.g., col. 12, lines 51-55, "plurality of input queues") at the choosing of originating subsystems each including a bus arbitration priority and being granted access to the bus (e.g., col. 10, lines 37-39, 14, "components ... for both directions") and the second state machine to service certain inbound queues according to first and second priorities (e.g., col. 11-14). While Brown thus expressly mentions first and second inbound queues of the single bus recited, and according priority to inbound queues, he does not expressly mention according priority to inbound queues which pertain to the single bus recited; however, Bergeson discloses this (e.g., Figs. 1b, 2a; col. 3, lines 13-27, adequately teaches according priority to inbound queues). It would have been obvious to one of ordinary skill in the art to combine Bergeson with Brown, because Bergeson teaches the advantage of managing priority on inbound queues (e.g., col. 1, lines 15-21). Brown does not expressly mention the bus as on-chip; however the Examiner takes Official Notice that the integration of circuits onto a chip is widely known to improve the speed and performance of the circuits, as evidenced by Geusic (para. 4).

Regarding claim 8, Brown also discloses storing priorities to be accorded in a configuration register (e.g., col. 11, lines 9-15, "target device basis").

Regarding claim 9, Brown also discloses a plurality of inbound queues (e.g., col. 12, lines 51-55, "plurality of input queues") at the choosing of originating subsystems

each including a bus arbitration priority and being granted access to the bus (e.g., col. 10, lines 37-39, 14, "components ... for both directions") and the second state machine also coupled to the additional inbound queue. Brown does not expressly mention according priority to the third inbound queues which pertain to the single bus recited, complementing the first and second inbound queue; however, Bergeson discloses this (e.g., Figs. 1b, 2a; col. 3, lines 13-27, adequately teaches according priority to inbound queues). It would have been obvious to one of ordinary skill in the art to combine Bergeson with Brown, because Bergeson teaches the advantage of managing priority on inbound queues (e.g., col. 1, lines 15-21). The plurality of inbound queues disclosed by Brown refers to two or more queues and thus encompasses a third inbound queue, which is not unforeseen, as seen by Brown, who teaches adding further additional queues to the existing two outbound queues to increment the granularity of prioritization (e.g., col. 10, lines 26-28), and by Bergeson, who teaches using three inbound queues, each accorded a priority (e.g., Fig. 2a, "202", "204", "206", col. 3, lines 13-27).

Regarding claim 17, Brown discloses core subsystem logic (e.g., col. 6, lines 41-47), the first and second inbound queues (e.g., col. 12, lines 51-55, "plurality of input queues") at the choosing of originating subsystems each including a bus arbitration priority and being granted access to the bus (e.g., col. 10, lines 37-39, 14, "components ... for both directions") and the second state machine to service certain inbound queues according to first and second priorities (e.g., col. 11-14). While Brown thus expressly mentions first and second inbound queues of the single bus recited, and according priority to inbound queues, he does not expressly mention according priority to inbound

queues which pertain to the single bus recited; however, Bergeson discloses this (e.g., Figs. 1b, 2a; col. 3, lines 13-27, adequately teaches according priority to inbound queues). It would have been obvious to one of ordinary skill in the art to combine Bergeson with Brown, because Bergeson teaches the advantage of managing priority on inbound queues (e.g., col. 1, lines 15-21).

Brown does not expressly mention the bus as on-chip; however the Examiner takes Official Notice that the integration of circuits onto a chip is widely known to improve the speed and performance of the circuits, as evidenced by Geusic (para. 4).

Regarding claim 18, Brown also discloses storing priorities to be accorded in a configuration register (e.g., col. 11, lines 9-15, "target device basis").

Regarding claim 19, Brown also discloses a plurality of inbound queues (e.g., col. 12, lines 51-55, "plurality of input queues") at the choosing of originating subsystems each including a bus arbitration priority and being granted access to the bus (e.g., col. 10, lines 37-39, 14, "components ... for both directions") and the second state machine also coupled to the additional inbound queue. Brown does not expressly mention according priority to the third inbound queues which pertain to the single bus recited, complementing the first and second inbound queue; however, Bergeson discloses this (e.g., Figs. 1b, 2a; col. 3, lines 13-27, adequately teaches according priority to inbound queues). It would have been obvious to one of ordinary skill in the art to combine Bergeson with Brown, because Bergeson teaches the advantage of managing priority on inbound queues (e.g., col. 1, lines 15-21). The plurality of inbound queues disclosed by Brown refers to two or more queues and thus encompasses a third inbound queue,

which is not unforeseen, as seen by Brown, who teaches adding further additional queues to the existing two outbound queues to increment the granularity of prioritization (e.g., col. 10, lines 26-28), and by Bergeson, who teaches using three inbound queues, each accorded a priority (e.g., Fig. 2a, "202", "204", "206", col. 3, lines 13-27).

Regarding claim 20, Brown also discloses a collection of peripheral device controllers (e.g., Fig. 5a, "550", "550").

Regarding claim 23, Brown also discloses staging transactions from other subsystems in a priority based manner as requested by originating subsystems of the transactions (e.g., col. 12, lines 51-55, "plurality of input queues"), and serially servicing the staged transactions from other subsystems (e.g., col. 10, lines 37-39, 14, "components ... for both directions") and notifying core logic of the subsystem in accordance with priorities (e.g., col. 11-14). Brown does not expressly mention according priority to inbound transactions which pertain to the single bus recited; however, Bergeson discloses this (e.g., Figs. 1b, 2a; col. 3, lines 13-27, adequately teaches according priority to inbound queues). It would have been obvious to one of ordinary skill in the art to combine Bergeson with Brown, because Bergeson teaches the advantage of managing priority on inbound queues (e.g., col. 1, lines 15-21).

Regarding claim 24, Brown also discloses staging each transaction in a selected one of a plurality of inbound queues (e.g., col. 12, lines 51-55, "plurality of input queues").

Regarding claim 25, Brown discloses staging transactions from other subsystems in a priority based manner as requested by originating subsystems (e.g., col. 11, lines

14-15, "initiator device basis"), and serially servicing the staged transactions from other subsystems, notifying core logic of the subsystem in accordance with the priority based manner from other subsystems are staged (e.g., col. 10, lines 11-13). Brown does not expressly mention according priority to inbound transactions which pertain to the single bus recited; however, Bergeson discloses this (e.g., Figs. 1b, 2a; col. 3, lines 13-27, adequately teaches according priority to inbound queues). It would have been obvious to one of ordinary skill in the art to combine Bergeson with Brown, because Bergeson teaches the advantage of managing priority on inbound queues (e.g., col. 1, lines 15-21). Brown does not expressly mention the bus as on-chip; however the Examiner takes Official Notice that the integration of circuits onto a chip is widely known to improve the speed and performance of the circuits, as evidenced by Geusic (para. 4).

Regarding claim 26, Brown also discloses staging each transaction in a selected one of a plurality of inbound queues (e.g., col. 12, lines 51-55, "plurality of input queues").

Regarding claim 27, Brown discloses a plurality of subsystems coupled to a bus interacting with each other through transactions (e.g., Fig. 5a, "523", "552", "225"), at least one of the data transfer interfaces allows the subsystem to initiate transactions in a prioritized manner (e.g., col. 11, lines 9-15) including a first intra-subsystem prioritization on the order transactions contending are to be serviced (e.g., col. 10, lines 10-13), and a second inter-subsystem prioritization on the order transactions are to be granted access to the bus (e.g., col. 10, lines 23-26). Brown does not expressly mention according priority to inbound queues which pertain to the single bus recited; however,

Bergeson discloses this (e.g., Figs. 1b, 2a; col. 3, lines 13-27, adequately teaches according priority to inbound queues). It would have been obvious to one of ordinary skill in the art to combine Bergeson with Brown, because Bergeson teaches the advantage of managing priority on inbound queues (e.g., col. 1, lines 15-21). Brown does not expressly mention the bus as on-chip; however the Examiner takes Official Notice that the integration of circuits onto a chip is widely known to improve the speed and performance of the circuits, as evidenced by Geusic (para. 4).

Regarding claim 28; Brown also discloses the generating and staging in a selected on of first and second outbound queues (e.g., Fig. 6, "631", "632"; col. 10, 26-28) in accordance with the determined intra-system priorities including with each a bus arbitration priority for use to arbitrate access (e.g., col. 10, lines 13-15).

Regarding claims 29 and 30, Brown also discloses first and second inbound queues (e.g., col. 12, lines 51-55, "plurality of input queues") at the choosing of originating subsystems each including a bus arbitration priority and being granted access to the bus (e.g., col. 10, lines 37-39, 14, "components ... for both directions") and the second state machine to service certain inbound queues according to first and second priorities (e.g., col. 11-14). While Brown thus expressly mentions first and second inbound queues of the single bus recited, and according priority to inbound queues, he does not expressly mention according priority to inbound queues which pertain to the single bus recited; however, Bergeson discloses this (e.g., Figs. 1b, 2a; col. 3, lines 13-27, adequately teaches according priority to inbound queues).

Regarding claim 31, Brown also discloses a collection of peripheral device controllers (e.g., Fig. 5a, "550", "550").

Regarding claim 32, Brown discloses a first subsystem (e.g., Fig. 4, "222") having a first data transfer interface interfacing the first subsystem to the bus, initiating first transactions with other subsystems to internally prioritize the order the first transactions are to be serviced by the first data transfer interface (e.g., col. 11, lines 11-15, "'data stream' basis"), and a second subsystem initiating second transactions to internally prioritizing the order the second transactions are to be serviced by the second data transfer interface and including priorities to facilitate prioritization of granting of access to the bus to contending transactions (e.g., col. 10, lines 23-26). Brown does not expressly mention first bus arbitration priorities to facilitate prioritization of granting of access to the on-chip bus to contending inter-subsystem transactions including the first transactions; however, Bergeson discloses this (e.g., col. 3, lines 13-19, "high priority" and "medium priority"). It would have been obvious to one of ordinary skill in the art to combine Bergeson with Brown, because Bergeson teaches the advantage of managing priority to facilitate granting access (e.g., col. 1, lines 15-21). Brown does not expressly mention the bus as on-chip; however the Examiner takes Official Notice that the integration of circuits onto a chip is widely known to improve the speed and performance of the circuits, as evidenced by Geusic (para. 4).

Regarding claim 33, Brown also discloses staging third transactions from other subsystems in a priority based manner as requested by originating subsystems (col. 10, lines 10-13) also having a third bus arbitration priority based on which accesses to said

bus were granted (col. 11, lines 33-35). Brown does not expressly mention according priority to inbound queues which pertain to the single bus recited; however, Bergeson discloses this (e.g., Figs. 1b, 2a; col. 3, lines 13-27, adequately teaches according priority to inbound queues).

Regarding claim 34, Bergeson also discloses serially servicing the staged third transaction notifying core logic of the first subsystem in accordance with the priority based manner in which they are staged (e.g., Fig. 2a, "202", "204", "206").

Regarding claim 35, Bergeson also discloses staging fourth transactions from other subsystems in a priority based manner as requested by originating subsystems, also having fourth bus arbitration priorities, based on which access to said bus were granted (e.g., col. 3, lines 12-16).

Response to Arguments

Applicant's arguments filed 7/18/05 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Elkhoury (US RE37980 E; Fig. 2), Rasmussen (US 6317803 B1; Fig. 2-2), Dahlen (US 20030189573 A1; Fig. 6), Pawlowski (US 5905876 A; Fig. 2, "10", "20", col. 5, lines 55-58, 62-66), Van Loo (US 5657472 A; Fig. 4), Comeau (US

20010049726 A1; Fig. 6, "263", "264") all disclose multiple inbound and outbound queues which bear some features of the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H. Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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